ABSTRACT

A microcomputer 11 with a debug circuit 11b implemented therein for realizing an on-chip debugging function is mounted on a target board 10 in which a variety of buses 15 are led out and connected to a break board 30. The break board 30 is provided with a break condition storage section 31 and a break signal generation section 32. Break conditions are written in the break condition storage section 31 from the side of a debugger 20 through the debug circuit 11b, the CPU 11a and the various buses 15. Then, a user program stored in a ROM 12 is executed. The break signal generation section 32 monitors signals on the various buses 15, and outputs a break generation signal 30a when the signals on the various buses 15 coincide with the break condition. The execution of the user program is interrupted (stopped) based on the break generation signal 30a.